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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,110	12/12/2003	Nathan R. Carter	A8SJ2357US	3653
23935 7	590 03/22/2005		EXAM	INER
•	COBS, PATRICK &	MOTTOLA, STEVEN J		
	555 ST. CHARLES DRIVE SUITE 107			PAPER NUMBER
	OAKS, CA 91360		2817	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		t i		
	Application No.	Applicant(s)		
	10/736,110	CARTER, NATHAN R.		
Office Action Summary	Examiner	Art Unit		
	Steven J. Mottola	2817		
The MAILING DATE of this communication a	appears on the cover sheet w	th the correspondence address		
A SHORTENED STATUTORY PERIOD FOR REI THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a - If NO period for reply is specified above, the maximum statutory peri - Failure to reply within the set or extended period for reply will, by state Any reply received by the Office later than three months after the material patent term adjustment. See 37 CFR 1.704(b).	N. 1.136(a). In no event, however, may a largely within the statutory minimum of thir lod will apply and will expire SIX (6) MON tute, cause the application to become Al	eply be timely filed y (30) days will be considered timely. THS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).		
Status				
1) Responsive to communication(s) filed on	·			
2a) ☐ This action is FINAL . 2b) ☑ T	his action is non-final.			
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits i				
closed in accordance with the practice unde	er <i>Ex parte Quayle</i> , 1935 C.D). 11, 453 O.G. 213.		
Disposition of Claims				
4) ⊠ Claim(s) 1-28 is/are pending in the applicating 4a) Of the above claim(s) is/are without 5) ⊠ Claim(s) 1,2 and 4-28 is/are allowed. 6) ⊠ Claim(s) 3 is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and	Irawn from consideration.			
Application Papers				
9) The specification is objected to by the Exam 10) The drawing(s) filed on is/are: a) a Applicant may not request that any objection to to Replacement drawing sheet(s) including the cord 11) The oath or declaration is objected to by the	accepted or b) objected to the drawing(s) be held in abeyal rection is required if the drawing	nce. See 37 CFR 1.85(a). (s) is objected to. See 37 CFR 1.121(d).		
Priority under 35 U.S.C. § 119				
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of: 1. Certified copies of the priority docume 2. Certified copies of the priority docume 3. Copies of the certified copies of the papplication from the International Bur * See the attached detailed Office action for a	ents have been received. ents have been received in A riority documents have been eau (PCT Rule 17.2(a)).	application No received in this National Stage		
Attachment(s) 1) Notice of References Cited (PTO-892)	4) ☐ Intonious	Summary (PTO-413)		
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/Paper No(s)/Mail Date 010204. 	Paper No(s)/Mail Date nformal Patent Application (PTO-152)		

Application/Control Number: 10/736,110

Art Unit: 2817

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is no antecedent basis for "said NPN and PNP diversion transistors" at lines 3-4 of the claim; by way of suggestion perhaps this claim was meant to depend from claim 2 rather than claim 1.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ryat discloses in fig. 2 complementary differential input stages each having a current source. Cross coupled between the current sources are diode loads that compensate for large common mode signals. Voorman et al. disclose complementary input pairs in fig. 1 for instance that each have a current source transistor coupled to their common emitters, and a pair of diode transistors coupled therebetween. The applicant is presumed familiar with his prior patent cited as Carter.

Claims 1-2 and 4-18 are allowed.

None of the references of record generate complementary currents to modulate the tail current as a function of the difference between the common emitter node voltages of the differential pair as required by claims 1 and 28 or using transistors having their bases connected to the respective common emitter nodes of the differential pairs to generate or divert such currents as a function of the voltage difference between the nodes as required by claims 4 and 24.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Mottola whose telephone number is 571-272-1766. The examiner can normally be reached on M-Th from 8 to 5. The examiner can also be reached on alternate Fridays from 8 to 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal, can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven J. Mottola